Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (currently amended). Apparatus comprising:

an inkjet print head chip having a silicon substrate and MOS logic blocks, resistor elements to heat the chip, and a controller of the resistor elements; and

temperature sense resistors implanted in the silicon substrate of the print head chip ~~by directing atoms of an implantation material toward the substrate and beneath the substrate surface~~ and comprising atoms of an implantation material, wherein the atoms of the implantation material are embedded beneath the substrate surface, the temperature sense resistors being operatively connected to the controller of the resistor elements to enable the controller to monitor the chip temperature to control the resistor elements to heat the chip.

2 (previously presented). The apparatus of claim 1, wherein the temperature sense resistors have a sheet resistance of at least 20 Ω/□ and a temperature coefficient of resistivity of at least 0.0010 Ω/°C.

3 (previously presented). The apparatus of claim 1, wherein the temperature sense resistors have a sheet resistance of at least 75 Ω/□ and a temperature coefficient of resistivity of at least 0.0020 Ω/°C.

4 (previously presented). The apparatus of claim 1, wherein the temperature sense resistors have a sheet resistance of at least 500 Ω/□ and a temperature coefficient of resistivity of at least 0.0030 Ω/°C.

5 (previously presented). The apparatus of claim 1, wherein the temperature sense resistors

have a sheet resistance of at least 1000 Ω/□ and a temperature coefficient of resistivity of at least 0.0040 Ω/°C

6 (previously presented). The apparatus of claim 1, wherein the temperature sense resistors comprise N-Well material.

7 (previously presented). The apparatus of claim 1, wherein the temperature sense resistors comprise NSD material.

8 (previously presented). The apparatus of claim 1, wherein the temperature sense resistors comprise LDD material.

9 (previously presented). The apparatus of claim 1, wherein the temperature sense resistors comprise PSD material.

10 (previously presented). The apparatus of any claim 1, wherein the inkjet print head chip includes 1 - 1000 temperature sense resistors.

11 (previously presented). The apparatus of claim 1, wherein each temperature sense resistor is 0.05 - 5000 μm wide by 0.01 - 400,000 μm long by 0.05 - 4 μm thick.

12 (previously presented). The apparatus of claim 1, wherein each temperature sense resistor is 1 - 2000 μm wide by 1 - 200,000 μm long by 0.1 - 3 μm thick.

13 (previously presented). The apparatus of claim 1, wherein each temperature sense resistor is 2 - 1000 μm wide by 2 - 100,000 μm long by 0.2 - 2 μm thick.

14 (previously presented). The apparatus of claim 1, further comprising an inkjet print head comprising the inkjet print head chip.

15 (original). The apparatus of claim 13, further comprising an ink jet printer comprising the inkjet print head.

16 (currently amended). A method of controlling the temperature of an inkjet print head chip having a substrate and MOS logic blocks, comprising:

providing the print head chip with at least one substrate heater to heat the chip;

providing the print head chip with a controller of the substrate heater;

implanting temperature sense resistors in the substrate of the chip, wherein the operation of implanting comprises directing a beam of energetic ions incident upon the substrate to embed those ions into the substrate;

operatively connecting the temperature sense resistors to the controller of the substrate heater to enable the controller to monitor the chip temperature to control the substrate heater to heat the chip; and

using the controller to control the substrate heater to heat the chip.

17 (previously presented). The method of claim 16, wherein the temperature sense resistors have a sheet resistance of at least 20 Ω/□ and a temperature coefficient of resistivity of at least 0.0010 Ω /°C.

18 (previously presented). The method of claim 16, wherein the temperature sense resistors have a sheet resistance of at least 75 Ω/□ and a temperature coefficient of resistivity of at least 0.0020 Ω /°C.

19 (previously presented). The method of claim 16, wherein the temperature sense resistors have a sheet resistance of at least 500 Ω/□ and a temperature coefficient of resistivity of at least 0.0030 Ω/°C.

20 (previously presented). The method of claim 16, wherein the temperature sense resistors have a sheet resistance of at least 1000 Ω/□ and a temperature coefficient of resistivity of at least 0.0040 Ω/°C

21 (previously presented). The method of claim 16, wherein the temperature sense resistors comprise N-Well material.

22 (previously presented). The method of claim 16, wherein the temperature sense resistors comprise NSD material.

23 (previously presented). The method of claim 16, wherein the temperature sense resistors comprise LDD material.

24 (previously presented). The method of claim 16, wherein the temperature sense resistors comprise PSD material.

25 (previously presented). The method of claim 16, wherein the inkjet print head chip includes 1 - 1000 temperature sense resistors.

26 (previously presented). The method of claim 16, wherein each temperature sense resistor is 0.05 - 5000 μm wide by 0.01 - 400,000 μm long by 0.05 - 4 μm thick.

27 (previously presented). The method of claim 16, wherein each temperature sense resistor is 1 - 2000 μm wide by 1 - 200,000 μm long by 0.1 - 3 μm thick.

28 (previously presented). The method of claim 16, wherein each temperature sense resistor is 2 - 1000 μm wide by 2 - 100,000 μm long by 0.2 - 2 μm thick.

29 (previously presented). The method of claim 16, further comprising installing the inkjet print head chip in an inkjet print head.

30 (original). The method of claim 29, further comprising installing the inkjet print head in an ink jet printer.

31 (previously presented). The invention of claim 16, wherein the MOS logic blocks are CMOS logic blocks.

32 (canceled).